FRAUNHOFER ENAS

Acceleration Sensor AC05G

Version   0.8
Date   April 24, 2018

Authors: Fraunhofer Institute for Electronic Nano
              Systems (ENAS)
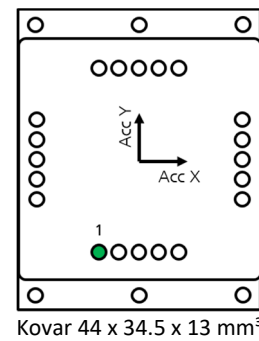   Electronic Design Chemnitz GmbH (EDC)

Kovar 44 x 34.5 x 13 mm³

Fig. 1: Package dimensions

The AC05G is a MEMS based 2-axis 5g accelerometer. It consists of the MEMS transducer, the read-out and control electronics (ASIC) and a printed circuit board with passive devices. All components are mounted into a commercial standard package. This type of package is used for demonstration and characterization of the sensor system. The accelerometer specification is summarized in Tab. 1. A schematic cross section of the sensor package and a photo of the MEMS and ASIC setup is shown in Fig. 2. The acceleration sensor is part of current research activities of Fraunhofer ENAS. The MEMS elements have been fabricated in the Center for Microtechnologies (ZfM) and the application specific integrated circuit (ASIC) has been designed by EDC.

Tab. 1: Acceleration sensor specification

Parameter	Sign	Value	Unit
Number of axes		2	
Measurement range	±	5	g
Scale Factor Nonlinearity	<	350	ppm
Bandwidth		500	Hz
Operation temperature range		-40…+85	°C
Shock resistance		50	g
Bias instability (BI)	<	100	µg
Velocity random walk (VRW)	<	0.15	m/s/√h
Noise	<	250	µg/√Hz
Power supply		5	Volt
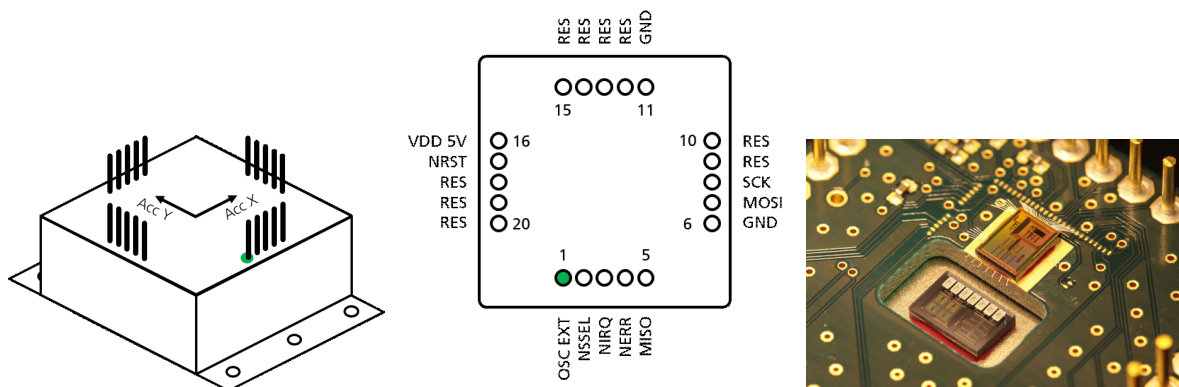
Fig. 2: Package drawing, pin description and photo of MEMS and ASIC setup

Fraunhofer
ENAS

Tab. 2: Pin description

| Pin#	Name	Remark		Pin#	Name	Remark
1	OSC EXT	External oscillator		11	GND	0 V supply
2	NSSEL	SPI		12	Reserved	Leave unconnected
3	NIRQ	SPI		13	Reserved	Leave unconnected
4	NERR	SPI		14	Reserved	Leave unconnected
5	MISO	SPI		15	Reserved	Leave unconnected
6	GND	0 V supply		16	VDD 5V	5 V supply
7	MOSI	SPI		17	NRST	System reset if set to GND
8	SCK	SPI		18	Reserved	Leave unconnected
9	Reserved	Leave unconnected		19	Reserved	Leave unconnected
10	Reserved	Leave unconnected		20	Reserved	Leave unconnected
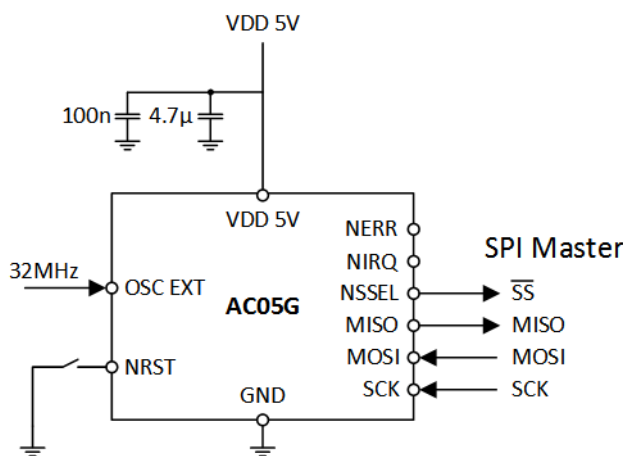
Fig. 3: Application diagram

1 Micromechanical Sensor Element

The AC05G is a micromechanical sensor for the measurement of linear accelerations in two directions. The silicon sensor element has been designed for a closed loop operation up to 5 g. The MEMS is a Glass-Si-Glass stack.

Fig. 4: Chip dimensions

1.1 Designed features

- Highly doped silicon (0,01 ... 0,05 Ωcm)
- Sensitive to linear accelerations in x and y directions
- Eigenfrequency 4000 Hz ± 15 %
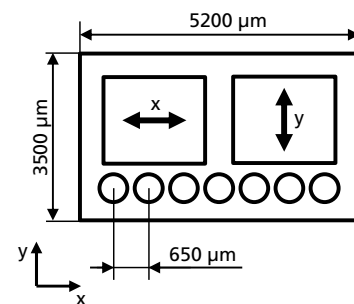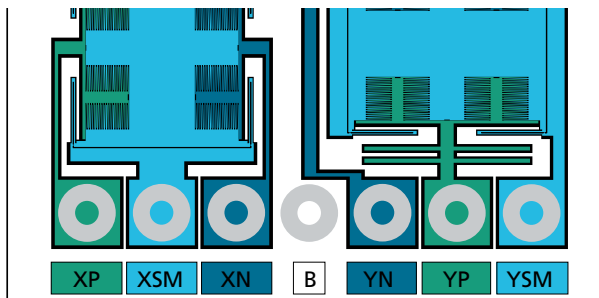- Damping ratio < 1
- Base capacitance per electrode < 10 pF

XP	Electrode in positive x-direction
XSM	Connection for seismic mass of x-sensing element
XN	Electrode in negative x-direction
B	Bulk connection
YN	Electrode in positive y-direction
YP	Electrode in negative y-direction
YSM	Connection for seismic mass of y-sensing element

Fig. 5: Connection scheme

2 Electronics

The necessary read-out and control electronics for the accelerometer is realized as a fully integrated mixed signal integrated circuit. It comprises of two main functional sections and certain support cells (Fig. 6):

- The analog front-end for capacitance to voltage conversion and control of the MEMS element.
- The digital module for further signal processing with a non-volatile memory and a trim unit. This module also contains the interface to the next signal processing level carried out as serial peripheral interface (SPI).
- The support cells of the ASIC are a temperature unit, a power on reset unit (POK), a voltage regulator and a reference voltage generator as well as a clock generator.

ASIC and MEMS have been co-designed to best fit to each other. Therefore, the ASIC design derives from the sensor specification and the physical properties of the chosen transducer.
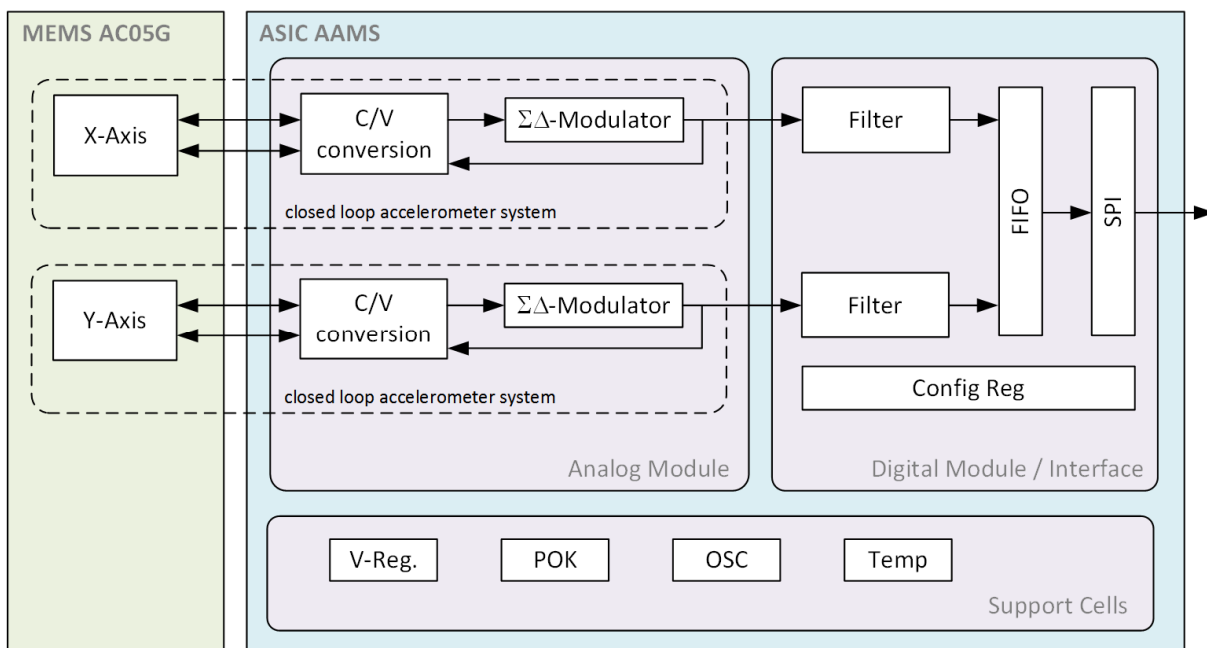

Fig. 6: Block diagram of the accelerometer system

3 SPI

3.1 Description

The ASIC contains an SPI slave interface. This interface is compatible to the SPI-Mode 0 (SCK-Default Low, Sampling with rising clock edge). 16 Bit Data are transferred with MSB first. Each data transmission will be triggered by sending of a SPI word by the host processor. This SPI word contains 1 Bit opcode (read or write), 7 Bit address and 8 Bit data. Writing of an 8 bit register is performed in one SPI cycle, writing of a 16- or 32-bit register requires two or four cycles, respectively. To read a register at least two cycles are necessary: The first cycle transfers the address to the ASIC, subsequent cycles receive the data from the ASIC and may trigger more read commands.

The internal registers of the ASIC may contain 32 Bit. Therefore, a hold register is implemented to keep the data integrity for the two SPI cycles, which are necessary to read a 32 Bit register. It is possible, to transfer the 16 MSB first as well as to transfer the 16 LSB first. A typical 32 Bit read access to a register needs 3 cycles: First: transfer the first address; Second: Transfer the second address and receive the first 16 bit of data; Third: receive the second 16 Bit of data.
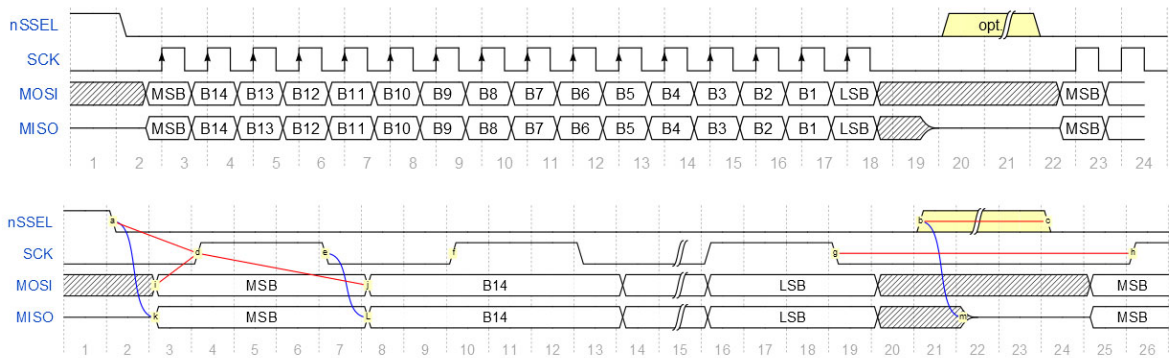
Fig. 7: SPI signal diagram

Tab. 3: SPI timing

Parameter		Meaning	Min	Typ	Max	Unit
t_{H_SCK}	d → e	Serial clock H-time	25	50	N/A	ns
t_{L_SCK}	e → f	Serial clock L-time	25	50	N/A	ns
t_{WAIT}	g → h	Wait between cycles / SCK must remain low	5/ f_{OSZ}			ns
t_{nSSEL}	b → c	NSSEL H between cycles / SCK must remain low	0			ns

For activation of the SPI, the signal nSSEL has to be set to Low. However, H-level between two SPI-accesses is not necessary. A bit counter controls the internal procedure of the SPI-machine. An H-level at nSSEL resets this bit counter and deactivates the MISO-Pin. Per definition SCK must remain Low at least 5 SYSCLK post last falling edge.

Fraunhofer
ENAS

Protocol/ Decoder:

MOSI - Register write (8 Bit)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	ADR(6:0)							DATA(7:0)							
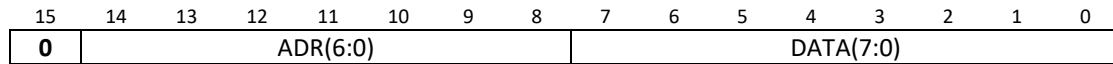
Write of the 8-Bit registers proceeds latest 5 system clocks post last falling edge at SCK.

MOSI - Register read (16 Bit)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	ADR(6:1)						x	Command							
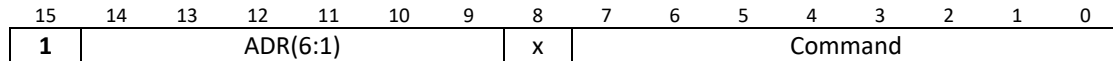
Data to read will be taken into hold register latest 5 system clocks post the last falling edge at SCK. The execution of an optional command proceeds latest 5 system clocks post the last falling edge at SCK as well. If no command should be executed the Bits 7:0 must have the value 0. The address bit ADR(0) will not be inquired.

Write 8 Bit

MOSI	0 / ADR / Data
MISO	any

Write 16 Bit

MOSI	0 / ADR / DATA (LSB)	0 / (ADR+1) / DATA (MSB)
MISO	any	any

Write 32 Bit

MOSI	0 / ADR / D0 (LSB)	0 / (ADR+1) / D1	0 / (ADR+2) / D2	0 / (ADR+3) / D3 (MSB)
MISO	any	any	any	any

Read 16 Bit

MOSI	1 / ADR / CMD	any
MISO	any	Read-Data

! Bit 0 of ADR will not be evaluated

Read 32 Bit

For 32 Bit read access the address has to be dividable by 4, both LSB of ADR are 0. The order of read is arbitrary (LSB first / MSB first).

MOSI	1 / ADR / CMD	1 / ADR+2 / CMD	any
MISO	any	Byte 1 / Byte 0	Byte 3 / Byte 2

or

MOSI	1 / ADR+2 / CMD	1 / ADR / CMD	any
MISO	any	Byte 3 / Byte 2	Byte 1 / Byte 0

! Bit ADR(0) will not be inquired, Bit ADR(1) must be 0.

3.2 FIFO

All periodically changed measurement data with time correlation will be sent via FIFO to SPI. Measurement data with a slow sampling rate (e.g. temperature) will be sent directly via the output multiplexer to SPI. In case of an overflow of the FIFO, a status bit will be set, which can only be reset by the user. The FIFO data contain a frequent counting value (6bit), which can be used for failure recognition of streaming failures. In case of an overflow, the read pointer will be incremented. Therefore, there is the possibility of inconsistent data sets in case of parallel reading via SPI. This will be covered by setting of an OVL bit in order to ignore the dataset. The control of the FIFO, will be executed by the digital ASIC-Core (new data signals of single measurement data) and by the user (Bit 2:0 of read command). If any data set is in the FIFO the nIRQ signal will pulled to Low level.

Tab. 4: FIFO commands

Command-Bit	Meaning
CMD-Bit 0 / Command 0x01	Release data set. Command has to be send when reading last Byte
CMD-Bit 1 / Command 0x02	Clear. All FIFO content will be cleared, OVL-Bit will be reset
CMD-Bit 2 / Command 0x04	Clear OVL
CMD-Bit 3 / Command 0x08	Activate FIFO. Command has to be sent before first reading. This command gives the main-software the control over the traffic via SPI regardless of lower software tasks (e.g. SPI ISR)
CMD-Bit 4 / Command 0x10	Deactivate FIFO. Command may be sent after last reading.
CMD-Bit 5 / Command 0x20	Lock FIFO Controls. OVL and empty Bits will be locked. This command must be set before reading first Byte of FIFO.

To read all FIFO data all addresses have to be sent with read command via SPI. In addition, at least the LOCK- and the RELEASE commands must be sent. The SPI word delay between transmitting an address and receiving the data word must considered.

Tab. 5: FIFO/SPI Example

Address	Command	SPI - MOSI	SPI MISO	Remark
Measure1	LOCK	0x0020	Any	
Measure3	-	0x0800	TSTAMP/FIFO	
Measure3	-	0x0A00	ACCEL X	
Measure4	-	0x0C00		
Measure4	RELEASE+ CLROVL	0x0E05	ACCEL Y	Release Dataset and update State-Bits for next Cycle
Dummy	NOP	0x3E00		Receive last Word from FIFO

![Fraunhofer ENAS]

3.3 Register and NVRAM content of Digital Interface- SPI slave

SPI register addressing

SPI-ADR	Name	MSB (8 Bit - ADR+1)	LSB (8 Bit - ADR+0)	Remark
0x00	MEASURE1		TSTAMP / FIFO-STATUS	FIFO behavior
0x02				
0x04	MEASURE2	ADC X MSB	ADC X LSB	FIFO behavior
0x06		ADC Y MSB	ADC Y LSB	FIFO behavior
0x08	MEASURE3	ACCEL X (LSB + 1)	ACCEL X (LSB)	FIFO behavior
0x0A		ACCEL X sign extension	ACCEL X (MSB)	FIFO behavior
0x0C	MEASURE4	ACCEL Y (LSB + 1)	ACCEL Y (LSB)	FIFO behavior
0x0E		ACCEL Y sign extension	ACCEL Y (MSB)	FIFO behavior
0x10	TEMPERAT	Temperature (MSB)	Temperature (LSB)	No FIFO
0x12		Temperature sign extension	Temperature sign extension	No FIFO
0x20	NVRAM	NVDATA	NVDATA	Only way to communicate
0x22		NVCMD | NVADR_HIGH	NVADR_LOW	with NVRAM
0x30	ASICID	ASIC-REV MSB	ASIC-REV LSB	ID-Register / SVN revision
0x32		0x43	0x51	Testpattern ,CP' + 1
0x38	SPITST	SPITST_Byte1	SPITST_Byte0	CMD0 inc bytes
0x3A		SPITST_Byte3	SPITST_Byte2	
0x3C				
0x3E		Free for last spi read cycle		

NVRAM addressing

NVRAM -ADR	Name	Purpose	Remark
0x000	CFG0	Basic- and Debug configuration	
0x020 / 0x021	LP0_B0	Lowpass stage 0 coefficient B0	
0x022 / 0x023	LP0_B1	Lowpass stage 0 coefficient B1	Little Endian 24 Bit:
0x024 / 0x025	LP0_B2	Lowpass stage 0 coefficient B2	Lower address contains 16 LSB of coefficient
0x026 / 0x027	LP0_A1	Lowpass stage 0 coefficient A1	Higher address contains 8 MSB of coefficient
0x028 / 0x029	LP0_A2	Lowpass stage 0 coefficient A2	
0x02A / 0x02B	LP1_B0	Lowpass stage 1 coefficient B0	
0x02C / 0x02D	LP1_B1	Lowpass stage 1 coefficient B1	
0x02E / 0x02F	LP1_B2	Lowpass stage 1 coefficient B2	
0x030 / 0x031	LP1_A1	Lowpass stage 1 coefficient A1	
0x032 / 0x033	LP1_A2	Lowpass stage 1 coefficient A2	
0x034 / 0x035	LP2_B0	Lowpass stage 2 coefficient B0	
0x036 / 0x037	LP2_B1	Lowpass stage 2 coefficient B1	
0x038 / 0x039	LP2_B2	Lowpass stage 2 coefficient B2	
0x03A / 0x03B	LP2_A1	Lowpass stage 2 coefficient A1	
0x03C / 0x03D	LP2_A2	Lowpass stage 2 coefficient A2	
0x03E / 0x03F	LPSCALE	Lowpass scale value	
0x1FF	VALIDATION	Validation of NVRAM content	0x4846 for valid NV content
0x3F0	TRIM GOX	Manufacture Trimming	
0x3F1	TRIM GOY	Manufacture Trimming	
0x3F2	TRIM MISC	Manufacture Trimming	
0x3FF	CPTRIM	Charge pump trim	FAB protected

Fraunhofer

ENAS

SPI register

MEASURE 1	Measurement FIFO state

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
								-							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			-							TSTAMP				OVL	EMP

Bit	Name	Reset	Format	Value	Meaning
31:8					
7:2	TSTAMP	0	Unsigned	TSTAMP	ASIC-Timestamp (FIFO behaviour)
1	OVL	0	Bit	0	No FIFO-Overflow, dataset valid
				1	Overflow, FIFO dataset loss, read dataset may be corrupt
0	EMP	1	Bit	0	Value in FIFO, dataset valid
				1	No values FIFO, read dataset invalid

MEASURE 2	Measurement FIFO

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
							ADCY								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							ADCX								

Bit	Name	Reset	Format	Value	Meaning
31:16	ADCY		Signed	ADCY	Amplitude y channel before filter
15:0	ADCX		Signed	ADCX	Amplitude x channel before filter

MEASURE 3	Measurement FIFO

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		ACCELX sign extension									ACCELX				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							ACCELX								

Bit	Name	Reset	Format	Value	Meaning
31:24	XSIGN		Signed	XSIGN	Sign extension. Register is readable as 32 bit signed
23:0	ACCELX		Signed	ACCELX	Acceleration x channel.

MEASURE 4	Measurement FIFO

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		ACCELY sign extension									ACCELY				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							ACCELY								

Bit	Name	Reset	Format	Value	Meaning
31:24	YSIGN		Signed	YSIGN	Sign extension. Register is readable as 32 bit signed
23:0	ACCELY		Signed	ACCELY	Acceleration y channel.

Fraunhofer

ENAS

TEMPERAT	Measurement FIFO

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
							Temperature sign extension								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							TEMP								
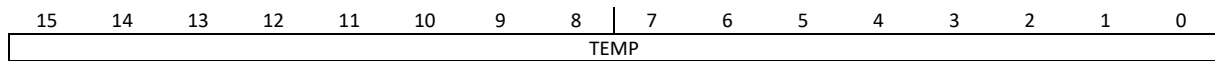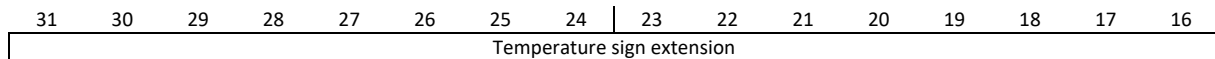
Bit	Name	Reset	Format	Value	Meaning
31:16	TSIGN		Signed	TSIGN	Sign extension. Register is readable as 32 bit signed
15:0	TEMP		Signed	TEMP	Temperature channel.

NVRAM	NVRAM and Configuration register access

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NVCMD			RST	-	TST					NVADR					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							NVDATA								
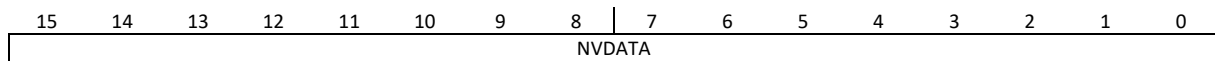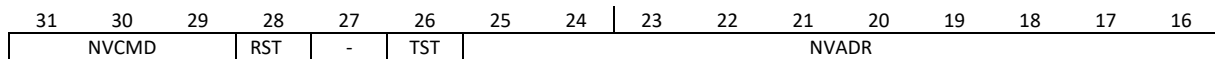
Bit	Name	Reset	Format	Value	Meaning
31:29	NVCMD		Bits		Command (write only), Address and write data must be valid
				001	Read SRAM cell of NVRAM
				010	Write SRAM cell of NVRAM and associated config.-register
				011	Copy SRAM cell to its associated configuration-register
				100	Recall NVRAM to SRAM (approx. 2.5 us)
				101	Store SRAM to NVRAM (approx. 25…30 ms)
28	RST	-	Command	0	Default value
				1	Forces software restart:
					→ RECALL NVRAM → Copy all content to register
					Remark: SPI access is not allowed during restart process
27					
26	TST		Bit	0	Default value
				1	In manufacture testmode:
					Writing of configuration registers only,
					NVRAM will not changed
25:16	NVADR		Unsigned		Adress to NVRAM (write only)
15:0	NVDATA		Unsigned		RAM Data

ASICREV	ASIC ID and code revision (read only)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
							ID								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							REV								
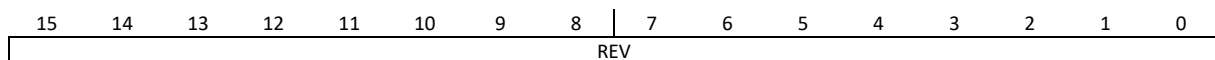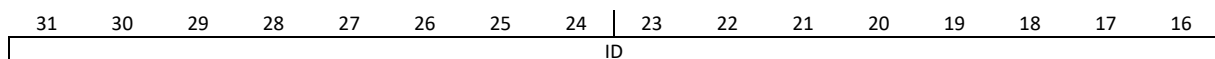
Bit	Name	Reset	Format	Value	Meaning
31:16	ID	0x4351	Unsigned	const	Unique EDC ASIC-ID ('CP' + 1)
15:0	REV	SVN	Unsigned	const	SVN number of ASIC code

Fraunhofer

ENAS

SPITST		SPI-Test

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
				SPIT3								SPIT2			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				SPIT1								SPIT0			

Bit	Name	Reset	Format	Value	Meaning
31:24	SPIT3	0xA4	Unsigned	N	Test value 3 It's incremented if the register is read with READCMD(0)=1
23:16	SPIT2	0x53	Unsigned	N	Test value 2 It's incremented if the register is read with READCMD(0)=1
15:8	SPIT1	0xA3	Unsigned	N	Test value 1 It's incremented if the register is read with READCMD(0)=1
7:0	SPIT0	0x51	Unsigned	N	Test value 0 It's incremented if the register is read with READCMD(0)=1

NVRAM register

CFG0		Config register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
											FIFODS				

Bit	Name	Reset	Format	Value	Meaning
7:0	FIFODS	32 (0x20)	unsigned	0 N 255	FIFO output rate is maximum (6.25kHz @ fosc=8MHz) FIFO output rate is f_{osz} / 1280 (1+N) FIFO output rate is minimum (24.5Hz @ fosc=8MHz)

LPx_Ay / LPx_By		Lowpass stage X, coefficient Ay / Lowpass stage X, coefficient By

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
												COEFF			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							COEFF								

Bit	Name	Reset	Format	Meaning
23:0	COEFF		Signed 24.22	Filtercoefficient

LPSCALE		Lowpass coefficient output scaler

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
												COEFF			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							COEFF								

Bit	Name	Reset	Format	Meaning
23:0	COEFF		Signed 24.21	Filtercoefficient

TRIM_GOX		gain and offset trim for X

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRIMGCX				TRIMOCTX					TRIMOCBX					

Bit	Name	Reset	Format	Value	Meaning
15:12	TRIMGCX	1111	bit	N	Trim value gain X
11:6	TRIMOCTX	000000	bit	N	Trim value offset top X
5:0	TRIMOCBX	000000	bit	N	Trim value offset bottom X

Fraunhofer

ENAS

TRIM_GOY	gain and offset trim for Y

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRIMGCY				TRIMOCTY						TRIMOCBY					

Bit	Name	Reset	Format	Value	Meaning
15:12	TRIMGCY	1111	bit	N	Trim value gain Y
11:6	TRIMOCTY	000000	bit	N	Trim value offset top Y
5:0	TRIMOCBY	000000	bit	N	Trim value offset bottom Y

TRIM_MISC	miscellaneous trim

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
										DP	TRIMOSC				

Bit	Name	Reset	Format	Value	Meaning
5	DP	0	bit	0	Enable digital testpads
				1	Disable digital testpads
4:0	TRIMOSC	00000	bit	N	Trim value internal oscillator